1. A method comprising:

writing pixel data to a first memory location;

performing a first pixel transformation at said first memory location;

generating a memory address for a second memory location; and

writing said transformed pixel data from said first memory location to said second memory location.

2. The method of claim 1 wherein writing pixel data to a first memory location includes writing pixel data to a first virtual memory location.

3. The method of claim 2 further including writing pixel data to a virtual memory location associated with a memory controller client that receives pixel data written to certain virtual addresses.

4. The method of claim 3 including causing an operating system to set aside virtual addresses for said memory controller client.

5. The method of claim 1 wherein entering an address for a second memory location includes transforming the addresses of said pixel data at said first memory location to addresses at said second memory location.

6. The method of claim 5 including determining the offset to each pixel data by subtracting a base address at said first memory location from the address of each pixel data.

7. The method of claim 6 including adding said offset to a base address of said second memory location.

8. The method of claim 1 wherein writing said transformed pixel data from said first memory location to said second memory location includes transferring said pixel data to a memory controller using a memory controller client.

9. The method of claim 1 wherein writing said transformed pixel data from said first memory location to said second memory location includes writing said pixel data from a first memory location associated with a first transfer function to a second memory location associated with a second transfer function.

10. The method of claim 9 including transforming the addresses of said pixel data from addresses in a first virtual memory range associated with said first transfer

function to memory addresses in a second virtual memory range associated with said second transfer function.

11. An article comprising a medium storing instructions that enable a processor-based system to:

write pixel data to a first memory location;

perform a first pixel transformation at said first memory location;

generate a memory address for a second memory location; and

write said transformed pixel data from said first memory location to said second memory location.

12. The article of claim 11 further storing instructions that enable the processor-based system to write pixel data to a first virtual memory location.

13. The article of claim 12 further storing instructions that enable the processor-based system to write pixel data to a virtual memory location associated with a memory controller client that receives pixel data written to certain virtual addresses.

14. The article of claim 13 further storing instructions that enable the processor-based system to

cause an operating system to set aside virtual addresses for said memory controller client.

15. The article of claim 11 further storing instructions that enable the processor-based system to transform the addresses of pixel data at said first memory location to addresses at said second memory location.

16. The article of claim 15 further storing instructions that enable the processor-based system to determine the offset to each pixel data by subtracting a base address at said first memory location from the address of each pixel data.

17. The article of claim 16 further storing instructions that enable the processor-based system to add said offset to a base address of said second memory location.

18. The article of claim 11 further storing instructions that enable the processor-based system to transfer said pixel data to a memory controller using a memory controller client.

19. The article of claim 11 further storing instructions that enable the processor-based system to

write said pixel data from a first memory location associated with a first transfer function to a second memory location associated with a second transfer function.

20. The article of claim 19 further storing instructions that enable the processor-based system to transform the addresses of said pixel data from addresses in a first virtual memory range associated with said first transfer function to memory addresses in a second virtual memory range associated with said second transfer function.

21. A system comprising:

a memory controller that receives pixel data and addresses;

a first memory controller client that forwards pixel data and addresses to a first transfer function; and

a second memory controller client that receives data from said first transfer function together with new addresses.

22. The system of claim 21 wherein said first controller client selectively forwards pixel data and addresses to one of a plurality of transfer functions and said second controller client receives pixel data with new addresses from a plurality of transfer functions.

23. The system of claim 22 wherein said memory controller client writes the pixel data back to said memory controller.

24. The system of claim 21 including a plurality of transfer functions, one of said transfer functions arranged to write output data to an address range of another transfer function.

25. The system of claim 24 wherein said transfer functions are associated with virtual memory address ranges.